IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Bu et al.

Docket No.: TI-36637

Serial No.: 10/810,905

Confirmation No.: 9390

Filed: 03/26/2004

Examiner: Stark, J. J.

Title: Improved CMOS Transistors and Methods of Forming Same

AMENDMENT UNDER 37 CFR §1.111

June 5, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the Office Action, dated 03/28/2006, in the above-identified patent application, please make the following amendments. They are respectfully submitted as a full and complete response to that Action. Charge any required fees to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor and an N-type dopant region to support a P-channel transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

forming a layer of insulating material over the lightly-doped extension regions;

forming an interfacial layer of nitrogen at the interface of the insulating layer and the lightly-doped extension regions;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks;

forming a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks;

annealing, with the capping layer in place, the extension and source and drain regions; and

removing the capping layer after the annealing.

2. (Original) The method of claim 1 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

3. (Original) The method of claim 1 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

4. (Original) The method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

5. (Original) The method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

6. (Original) The method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

7. (Original) The method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

8. (Original) The method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

9. (Original) The method of claim 1 wherein said gate stack further includes a nitride sidewall deposited with a BTBAS precursor.

10. (Original) A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor and a P-type dopant region to support a NMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

forming a layer of silicon oxide over the lightly-doped extension regions;

forming an interfacial layer of nitrogen between the lightly-doped extension regions and the silicon oxide layer, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3;

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks;

annealing, with the capping layer in place, the extension and source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and

removing the nitride cap after the annealing.

11. (Withdrawn) A semiconductor structure formed in the process of fabricating a CMOS transistor structure prior to an activating anneal, comprising:

a semiconductor substrate having an P-type dopant region to support an NMOS transistor and a N-type dopant region to support a PMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

a layer of insulating material over the semiconductor substrate and gate stack;

lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

an interfacial layer of nitrogen formed at the interface of the lighted-doped extension regions and the layer of insulating material;

source and drain regions in the semiconductor substrate adjacent to each of the gate stacks; and

a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks.

12. (Withdrawn) The structure of claim 11 wherein the layer of insulating material is silicon oxide.

13. (Withdrawn) The structure of claim 11 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

14. (Withdrawn) The structure of claim 11 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

15. (Withdrawn) The structure of claim 11 wherein the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

16. (Withdrawn) The structure of claim 11 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

17. (Withdrawn) The structure of claim 11 wherein the gate stack further includes a nitride sidewall deposited with BTBAS precursor.

18. (Withdrawn) A structure formed in the fabrication of a CMOS transistor semiconductor chip prior to an activating thermal anneal, comprising:

a semiconductor substrate having a P-type dopant region to support an NMOS transistor and an N-type dopant region to support a PMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate supporting an oxide sidewall;

lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

a layer of silicon oxide over the lightly doped extension regions;

an interfacial layer of nitrogen at the interface between the layer of silicon oxide and the lightly-doped extension regions, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent;

source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3; and

a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks.

REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove. Claims 1-10 are pending and rejected.

Independent Claim 1 positively recites annealing, with the capping layer in place, the extension and source and drain regions . These advantageously claimed features are not taught or suggested by the patents of Bu et al. and Iwasaki; either alone or in combination.

Bu et al. does not teach the advantageously claimed invention because Bu et al. does not teach annealing, with the capping layer in place, the extension and source and drain regions (column 4 lines 12-18). Similarly, Iwasaki does not teach the advantageously claimed invention because Iwasaki does not teach annealing, with the capping layer in place, the extension and source and drain regions (column 8 lines 18-25). Therefore, the combination of Bu et al. and Iwasaki does not teach annealing, with the capping layer in place, the extension and source and drain regions, as advantageously claimed

The Applicants respectfully traverse the statement on page 5 of the Office Action that "it would have been obvious to combine Iwasaki with Bu to obtain the

invention as specified." The Applicants submit that those of ordinary skill in the art would not combine a method of fabricating GaAs MES FET transistors (Iwasaki) with a method for fabricating a CMOS transistor (Bu et al.) because the process parameters are mutua lly exclusive (e.g. materials used, precursors used, temperatures used, etc.). Moreover, Iwasaki teaches away from the advantageously claimed invention because Iwasaki teaches that an anneal is performed "while" a film "is formed" as the protective film 35 (column 8 lines 18-25). Therefore, Iwasaki does not teach annealing with the capping layer in place as advantageously claimed.

Regarding Claim 6, the Applicants respectfully traverse the statement in the Office Action (page 6) that in column 3 lines 3-62 that Bu et al. teaches forming an interfacial layer of nitrogen by using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation. The Applicants submit that Bu et al. teaches the formation of a silicon oxynitride layer by a vapor deposition process (column 3 lies 35-54).

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over Bu et al. and Iwasaki; either alone or in combination. Furthermore, Claims 2-9 are allowable for depending on allowable independent Claim 1 and, in

combination, including limitations not taught or described in the reference s of record.

Independent Claim 10 positively recites annealing, with the capping layer in place, the extension and source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds. These advantageously claimed features are not taught or suggested by the patents of Bu et al. and Iwasaki; either alone or in combination.

Bu et al. does not teach the advantageously claimed invention because Bu et al. does not teach annealing, with the capping layer in place, the extension and source and drain regions (column 4 lines 12-18). Similarly, Iwasaki does not teach the advantageously claimed invention because Iwasaki does not teach annealing, with the capping layer in place, the extension and source and drain regions (column 8 lines 18-25). Therefore, the combination of Bu et al. and Iwasaki does not teach annealing, with the capping layer in place, the extension and source and drain regions, as advantageously claimed.

The Applicants respectfully traverse the statement on page 5 of the Office Action that "it would have been obvious to combine Iwasaki with Bu to obtain the invention as specified." The Applicants submit that those of ordinary skill in the art would not combine a method of fabricating GaAs MES FET t ransistors (Iwasaki)

with a method for fabricating a CMOS transistor (Bu et al.) because the process parameters are mutually exclusive (e.g. materials used, precursors used, temperatures used, etc.). Moreover, Iwasaki teaches away from the advantageously claimed invention because Iwasaki teaches that an anneal is performed "while" a film "is formed" as the protective film 35 (column 8 lines 18-25). Therefore, Iwasaki does not teach annealing with the capping layer in place as advantageously claimed.

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 10 and respectfully assert that Claim 10 is patentable over Bu et al. and Iwasaki; either alone or in combination.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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